SON-1199/CON PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Continuation Patent
Application of 08/968,456

Hideaki KURODA Group Art Unit: 2822

Application No. to be assigned Examiner: M. Prenty

Filed: May 29, 2001

For: SEMICONDUCTOR DEVICE
HAVING THREE CONNECTION HOLES
(as amended)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The present application is a continuation of the Patent Application No. 08/968,456 filed November 12, 1997. Prior to an initial examination of the above-identified patent application, please amend the application as follows:

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 7, with the following rewritten paragraph:

--The present invention relates to a semiconductor device and a method of manufacturing the same, and, more particularly, to a structure of a contact portion for taking out a conductive layer pattern of a diffusion layer, a wiring layer, etc. located at a deep position of the semiconductor device and a method of manufacturing the same.--

Please replace the paragraph beginning on page 3, line 20, with the following rewritten paragraph:

--Next, a plan view of the COP type DRAM cell will be shown in Fig. 2. Gate electrodes 51a to 51d of selection transistors 56a to 56g are arranged in parallel. Bit lines 53a to 53c connected to the diffusion layers of these selections transistors 56a to 56g by bit 52 are arranged orthogonal to the gate electrode 51 a to 51d. Th diffusion of the selection transistors 56a to 56g are provided with node contacts 54a to 54d connected to (not illustrated) capacitors. A sectional view taken along a A-A' of the figure is given in Fig. 3, and a sectional view taken along a line B-B' of the figure is given in Fig. 17. As seen from these sectional views, the node contacts 54a to 54d are "middle takeout contacts" using "pad-equipped" plugs. This DRAM is a COB type in which a bit line is a buried in the inter-layer insulating film between a selection transistor STr and a capacitor CAP. Further, the sectional view of Fig. 17 shows also a DRAM cell portion and a partial peripheral circuit.--

Please replace the paragraph beginning on page 4, line 14, with the following rewritten paragraph:

--Next, a simple explanation will be made of the method of manufacture of the COB type DRAM cell shown in Fig. 17 of a second related art by referring to Fig. 4 to Fig. 17. First, as shown in Fig. 4, an element isolation oxide film 120 is formed on a P type silicon substrate in which an N well and a P well are formed so to perform element isolation, then a (not illustrated) gate insulating film is formed by a thermal oxidation method, polysilicon 131a and tungsten silicide 131b are laminated, then patterning is carried out to form a gate electrode 131. Ion implantation is carried out by using this gate electrode 131 as a mask to form a lightly doped drain (LLD) 101.--

Please replace the paragraph beginning on page 19, line 14, with the following rewritten paragraph:

--To achieve the first object, in the semiconductor device, a conductive layer pattern is formed on a substrate and a inter-layer insulating film covering this conductive layer pattern is formed on the substrate. A first connection hole is formed in an upper layer of the inter-layer insulating film above the conductive layer pattern. Further, in this inter-layer insulating film, a second connection hole which reached the conductive layer pattern from the bottom portion of the first connection hole and has a smaller diameter than that of the first connection hole is formed. Further, a conductive plug is formed with the interior of the first connection hole and the second connection hole filled.--

Please replace the paragraph beginning on page 11, line 6, with the following rewritten paragraph:

--In the semiconductor device, the diameter of the connection hole formed in the upper portion is made larger than the second connection hole, and the conductive plug is formed in the first and second connection holes so as to fill them. Therefore, the diameter of the upper portion of this plug becomes larger then the diameter of the second connection hole.--

Please replace the paragraph beginning on page 14, line 13, with the following rewritten paragraph:

--In the method of manufacturing of the semiconductor device, after the first connection hole is formed in the upper layer of the inter-layer insulating film above the conductive layer pattern, the side wall is formed on the side wall of this first connection hole, and further the second connection hole is formed in the inter-layer insulating film by self-alignment in a state where it is communicated with the conductive layer pattern from the bottom portion of the first connection hole and where the diameter is smaller than that of the first connection hole by utilizing the side wall as a mask. Therefore, the second connection hole having a smaller diameter than that of the first connection hole is formed by only one masking step. The conductive plug is filled in the first connection hole and the second connection hole. Therefore, the diameter of the upper portion of the plug becomes larger than the diameter of the second connection hole.--

Please replace the paragraph beginning on page 16, line 22, with the following rewritten paragraph:

--Fig. 35 to Fig, 56 are sectional views explaining a first step for manufacturing a COB type DRAM according to a third embodiment of the present invention.--

Please replace the paragraph beginning on page 19, line 13, with the following rewritten paragraph:

--In the semiconductor device, the diameter of the first connection hole 216 formed at the upper portion is formed larger than that of the second connection hole 217, then the conductive plug 218 is formed in the first and second connection holes 216

and 217 in a state filling them. Therefore, the diameter of the upper portion of this plug 218 becomes larger than the diameter of the part of the plug 218 filled in the second connection hole 217.--

Please replace the paragraph beginning on page 20, line 12, with the following rewritten paragraph:

--Further, in the configuration wherein the conductive plug 218 is formed in a state filling the first and second connection holes 216 and 217 and the upper surface of this plug 218 is formed to almost the same height as the surface of the first inter-layer insulating film 215 where the film is formed on the surface of the first inter-layer insulating film 215, the coverage of the film becomes good and, at the same time, no step difference in formed in the lithography step after this, therefore the patterning precision is enhanced.--

Please replace the paragraph beginning on page 22, line 21, with the following rewritten paragraph:

--Then, as shown in Fig. 21, a side wall forming film 232 is formed on the inner wall of the first connection hole 216 and the first film 231. This side wall forming film 232 is formed, for example, a doped polysilicone. Subsequently, the part of the side wall forming film 232 indicated by a two dotted chain line is etched back to form the side wall 233 on the side wall of the first connection hole 216 by the side wall forming film 232.--

Please replace the paragraph beginning on page 25, line 16, with the following rewritten paragraph:

--Next, as shown in Fig. 26, a side wall forming film 243 is formed on the inner wall of the aperture 242 and the third film 241. This side wall forming film 243 is formed buy, for example, a doped polysilicon. Subsequently, by etch back the part of the side wall forming film 243 indicated by the two dotted chain line, a side wall 244 is formed on the side wall of the aperture 242 by this side wall forming film 242.--

Please replace the paragraph beginning on page 26, line 24, with the following rewritten paragraph:

--In the method of manufacture of the semiconductor device, the first connection hole 216 is formed in the upper layer of the first inter-layer insulating film 215 above the conductive layer pattern 214a, and further the second connection hole 217 is formed in the first inter-layer insulating film 215 in a state where it is communicated with the conductive layer pattern 214a from the bottom portion of the first connection hole 216 and has a smaller diameter than that of the first connection hole 216. Therefore, the first connection hole 216 formed in the upper portion is formed to have a larger diameter than that of the second connection hole 217. Them since the conductive plug 218 is

formed so as to be filled in the first and second connection holes 216 and 217, the diameter of the upper portion of the plug 218 becomes larger than the diameter of the second connection hole 217. The part having a diameter larger than the diameter of the second connection hole 217 becomes the pad 218A.--

Please replace the paragraph beginning on page 28, line 3, with the following rewritten paragraph:

--Further, the first film 231m the side wall 233, and the plug forming film 234 in the upper portion are removed from the surface of the first inter-layer insulating film 215 by etch back or CMP, and the plug 218 is formed in the first and second connection holes 216 and 217. Therefore, the upper surface of this plug 218 is formed to almost the same height as that of the surface of the first inter-layer insulating film 215. For this reason, the coverage of the second inter-layer insulating film 219 after this becomes good and, at the same time, although not illustrated, when forming the pattern on the second inter-layer insulating film 219, the lithography step can be carried out on the flat surface, therefore the patterning precision is enhanced.--

IN THE CLAIMS

Please cancel claims 1, 2 and 7-22 without prejudice or disclaimer.

3. (Amended, now includes subject matter of claim 1)

A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; and

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole;

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive portion which is connected to said plug and formed in said third connection hole.

4. (Amended, contains subject matter of claims 1 and 2)

A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; and

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole;

wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive contact portion which is connected to said plug and formed in said third connection hole.

5. (Amended) A semiconductor device according to claim 3, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

6. (Amended) A semiconductor device according to claim 4, wherein said plug and said conductive portion are a storage node contact portion of a dynamic random access memory.

REMARKS

This is a voluntary preliminary amendment directed to claims 3-6 of the parent application and amended by preliminary amendment. No further changes are made to these claims. Reexamination and reconsideration are respectfully requested for claims 3-6.

This preliminary amendment cancels claims 1, 2 and 7-22 that were allowed in the parent application. It is requested that the art cited and made of record in the parent application be considered in this divisional application.

Entry of the foregoing amendment prior to examination is respectfully requested. An early and favorable action on the material is respectfully requested. Should there be any questions regarding the application, the Examiner is invited to telephone the undersigned at telephone number listed below.

Respectfully submitted,

DATE: May 30, 2001

Ronald P. Kananen
Registration No. 24,104

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APPENDIX

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 1, line 7, with the following rewritten paragraph:

--The present invention relates to a semiconductor device and a method of manufacturing the same, [more particularly] and, more particularly, to a structure of a contact portion for taking out a conductive layer pattern of a diffusion layer, a wiring layer, etc. located at a deep position of the semiconductor device and a method of manufacturing the same.--

Please replace the paragraph beginning on page 3, line 20, with the following rewritten paragraph:

--Next, a plan view of the COP type DRAM cell will be shown in Fig. 2. Gate electrodes 51a to 51d of selection transistors 56a to 56g are arranged in parallel. Bit lines 53a to 53c connected to the diffusion layers of these selections transistors 56a to 56g by bit 52 are arranged orthogonal to the gate electrode 51 a to 51d. Th diffusion of the selection transistors 56a to 56g are provided with node contacts 54a to 54d connected to [not illustrated] (not illustrated) capacitors. A sectional view taken along a A-A' of the figure is given in Fig. 3, and a sectional view taken along a line B-B' of the figure is given in Fig. 17. As seen from these sectional views, the node contacts 54a to 54d are "middle takeout contacts" using "pad-equipped" plugs. This DRAM is a COB type in which a bit line is a buried in the inter-layer insulating film between a selection transistor STr and a capacitor CAP. Further, the sectional view of Fig. 17 shows also a DRAM cell portion and a partial peripheral circuit.--

Please replace the paragraph beginning on page 4, line 14, with the following rewritten paragraph:

--Next, a simple explanation will be made of the method of manufacture of the COB type DRAM cell shown in Fig. 17 of a second related art by referring to Fig. 4 to Fig. 17. First, as shown in Fig. 4, an element isolation oxide film 120 is formed on a P type silicon substrate in which an N well and a P well are formed so to perform element isolation, then a [not illustrated] (not illustrated) gate insulating film is formed by a thermal oxidation method, polysilicon 131a and tungsten silicide 131b are laminated, then patterning is carried out to form a gate electrode 131. Ion implantation is carried out by using this gate electrode 131 as a mask to form a lightly doped drain (LLD) 101.--

Please replace the paragraph beginning on page 19, line 14, with the following rewritten paragraph:

--[Namely, to] To achieve the first object, in the semiconductor device, a conductive layer pattern is formed on a substrate and a inter-layer insulating film covering this conductive layer pattern is formed on the substrate. A first connection hole is formed in an upper layer of the inter-layer insulating film above the conductive layer pattern. Further, in this inter-layer insulating film, a second connection hole which reached the conductive layer pattern from the bottom portion of the first connection hole and has a smaller diameter than that of the first connection hole is formed. Further, a conductive plug is formed with the interior of the first connection hole and the second connection hole filled.--

Please replace the paragraph beginning on page 11, line 6, with the following rewritten paragraph:

--In the semiconductor device, the diameter of the connection hole formed in the upper portion is made larger than the second connection hole, and the conductive plug is formed in the first and second connection holes so as to fill [them, therefore] them. Therefore, the diameter of the upper portion of this plug becomes larger then the diameter of the second connection hole.--

Please replace the paragraph beginning on page 14, line 13, with the following rewritten paragraph:

--In the method of manufacturing of the semiconductor device, after the first connection hole is formed in the upper layer of the inter-layer insulating film above the conductive layer pattern, the side wall is formed on the side wall of this first connection hole, and further the second connection hole is formed in the inter-layer insulating film by self-alignment in a state where it is communicated with the conductive layer pattern from the bottom portion of the first connection hole and where the diameter is smaller than that of the first connection hole by utilizing the side wall as a [mask, therefore] mask. Therefore, the second connection hole having a smaller diameter than that of the first connection hole is formed by only one masking step. The conductive plug is filled in the first connection hole and the second connection [hole, therefore] hole. Therefore, the diameter of the upper portion of the plug becomes larger than the diameter of the second connection hole.--

Please replace the paragraph beginning on page 16, line 22, with the following rewritten paragraph:

--Fig. 35 to Fig, [49]56 are sectional views explaining a first step for manufacturing a COB type DRAM according to a third embodiment of the present invention.--

Please replace the paragraph beginning on page 19, line 13, with the following rewritten paragraph:

--In the semiconductor device, the diameter of the first connection hole 216 formed at the upper portion is formed larger than that of the second connection hole 217, then the conductive plug 218 is formed in the first and second connection holes 216 and 217 in a state filling [them, therefore]them. Therefore, the diameter of the upper portion of this plug 218 becomes larger than the diameter of the part of the plug 218 filled in the second connection hole 217.--

Please replace the paragraph beginning on page 20, line 12, with the following rewritten paragraph:

--Further, in the configuration wherein the conductive plug 218 is formed in a state filling the first and second connection holes 216 and 217 and the upper surface of this plug 218 is formed to almost the same height as the surface of the first inter-layer insulating film 215 where the film is formed on the surface of the first inter-layer insulating film 215, the coverage of the film becomes good and, at the same time, no step difference in [not] formed in the lithography step after this, therefore the patterning precision is enhanced.--

Please replace the paragraph beginning on page 22, line 21, with the following rewritten paragraph:

--Then, as shown in Fig. 21, a side wall forming film 232 is formed on the inner wall of the first connection hole 216 and the first film 231. This side wall forming film 232 is formed by[for example], for example, a doped polysilicone. Subsequently, the part of the side wall forming film 232 indicated by a two dotted chain line is etched back to form the side wall 233 on the side wall of the first connection hole 216 by the side wall forming film 232.--

Please replace the paragraph beginning on page 25, line 16, with the following rewritten paragraph:

--Next, as shown in Fig. 26, a side wall forming film 243 is formed on the inner wall of the aperture 242 and the third film 241. This side wall forming film 243 is formed buy [for example], for example, a doped polysilicon. Subsequently, by etch back the part of the side wall forming film 243 indicated by the two dotted chain line, a side wall 244 is formed on the side wall of the aperture 242 by this side wall forming film 242.--

Please replace the paragraph beginning on page 26, line 24, with

the following rewritten paragraph:

--In the method of manufacture of the semiconductor device, the first connection hole 216 is formed in the upper layer of the first inter-layer insulating film 215 above the conductive layer pattern 214a, and further the second connection hole 217 is formed in the first inter-layer insulating film 215 in a state where it is communicated with the conductive layer pattern 214a from the bottom portion of the first connection hole 216 and has a smaller diameter than that of the first connection hole [216', therefore]216. Therefore, the first connection hole 216 formed in the upper portion is formed to have a larger diameter than that of the second connection hole 217. Them since the conductive plug 218 is formed so as to be filled in the first and second connection holes 216 and 217, the diameter of the upper portion of the plug 218 becomes larger than the diameter of the second connection hole 217. The part having a diameter larger than the diameter of the second connection hole 217 becomes the pad 218A.--

Please replace the paragraph beginning on page 28, line 3, with the following rewritten paragraph:

--Further, the first film 231m the side wall 233, and the plug forming film 234 in the upper portion are removed from the

surface of the first inter-layer insulating film 215 by etch back or CMP, and the plug 218 is formed in the first and second connection holes 216 and [217, therefore]217. Therefore, the upper surface of this plug 218 is formed to almost the same height as that of the surface of the first inter-layer insulating film 215. For this reason, the coverage of the second inter-layer insulating film 219 after this becomes good and, at the same time, although not illustrated, when forming the pattern on the second inter-layer insulating film 219, the lithography step can be carried out on the flat surface, therefore the patterning precision is enhanced.--

IN THE CLAIMS

3. (Amended, now includes subject matter of claim 1) [A semiconductor device according to claim 1,]
A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and

then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; and

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole;

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive portion which is connected to said plug and formed in said third connection hole.

4. (Amended, contains subject matter of claims 1 and 2) [A semiconductor device according to claim 2, wherein provision is made of]:

A semiconductor device, comprising:

a conductive layer pattern formed on a substrate;

an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate;

a first connection hole formed in a upper layer of said inter-layer insulating film above said conductive layer pattern;

a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection

hole and formed on said inter-layer insulation film; and

a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole;

wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film

an upper insulating film formed on said inter-layer insulating film;

a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and

a conductive contact portion which is connected to said plug and formed in said third connection hole.

5. (Amended) A semiconductor device according to claim 3, wherein said plug and said conductive portion are [the] a storage node contact portion of a dynamic random access memory.

6. (Amended) A semiconductor device according to claim 4, wherein said plug and said conductive portion are [the] a storage node contact portion of a dynamic random access memory.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Continuation Patent Application of 08/968,456

Hideaki KURODA

Application No. to be assigned

Filed: May 29, 2001

For: SEMICONDUCTOR DEVICE HAVING THREE CONNECTION HOLES (as amended)

Group Art Unit: 2822

Examiner: M. Prenty

LETTER TO OFFICIAL DRAFTSPERSON AND SUBMISSION OF COPRRECTED FORMAL DRAWING

Box Issue Fee
Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant seeks approval to amend Figs.1-17 of the drawings, as shown in red ink on the attached sheetS. Specifically, these figures are now clearly labeled Prior Art. Formal drawings incorporating these changes are enclosed.

Respectfully submitted,

DATE: May 30, 2001

Ronald P. Kananen
Registration No. 24,104

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FIG. 1(1)

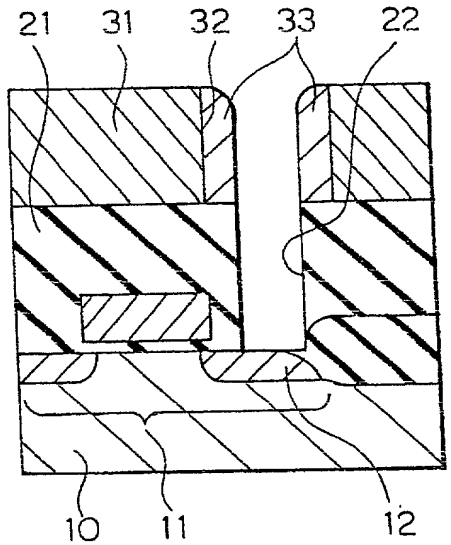


FIG. 1(2)

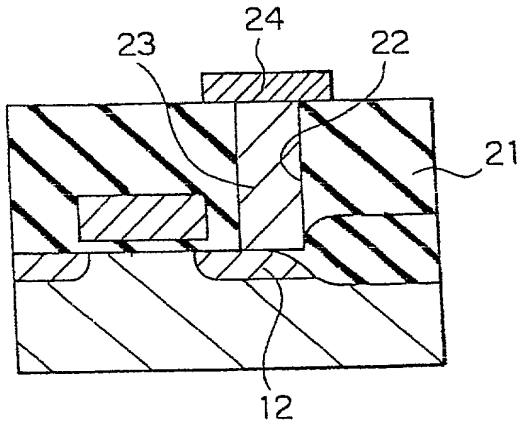
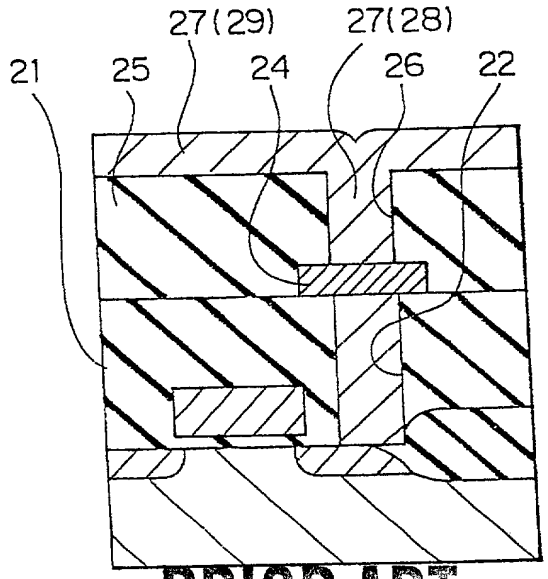


FIG. 1(3)



PRIOR ART

FIG. 2
PRIOR ART

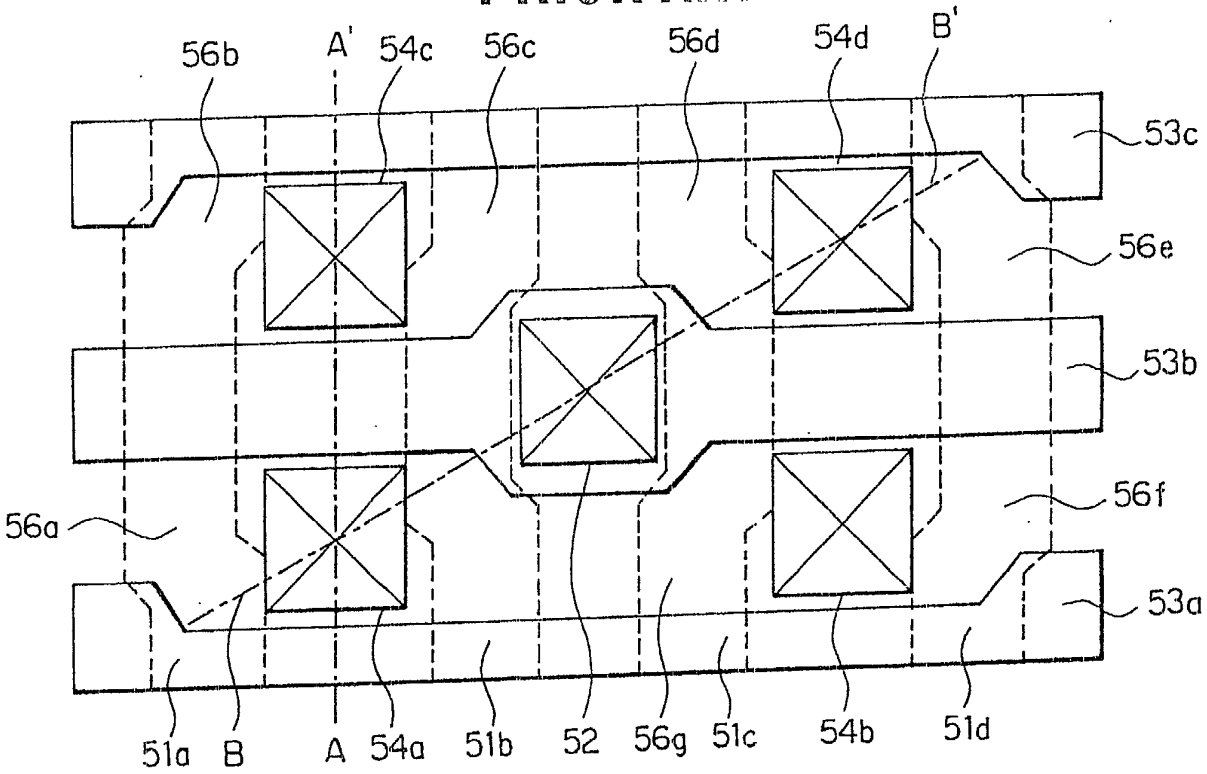


FIG. 3
PRIOR ART

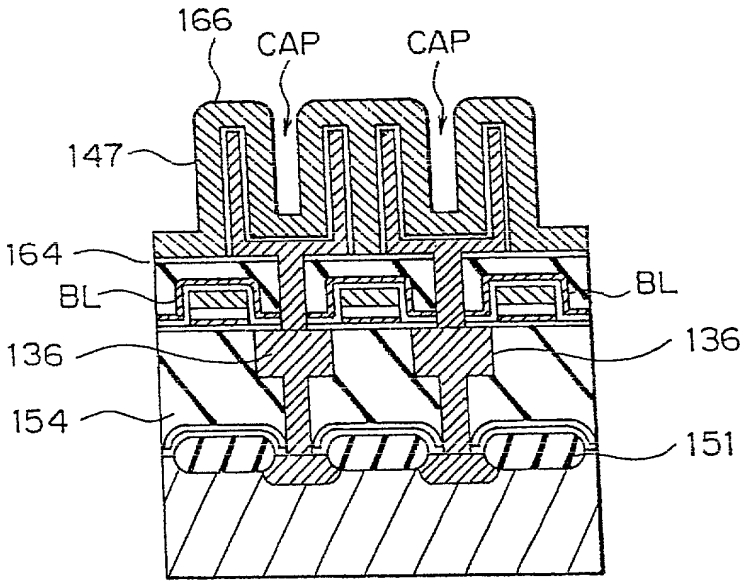


FIG. 4
PRIOR ART

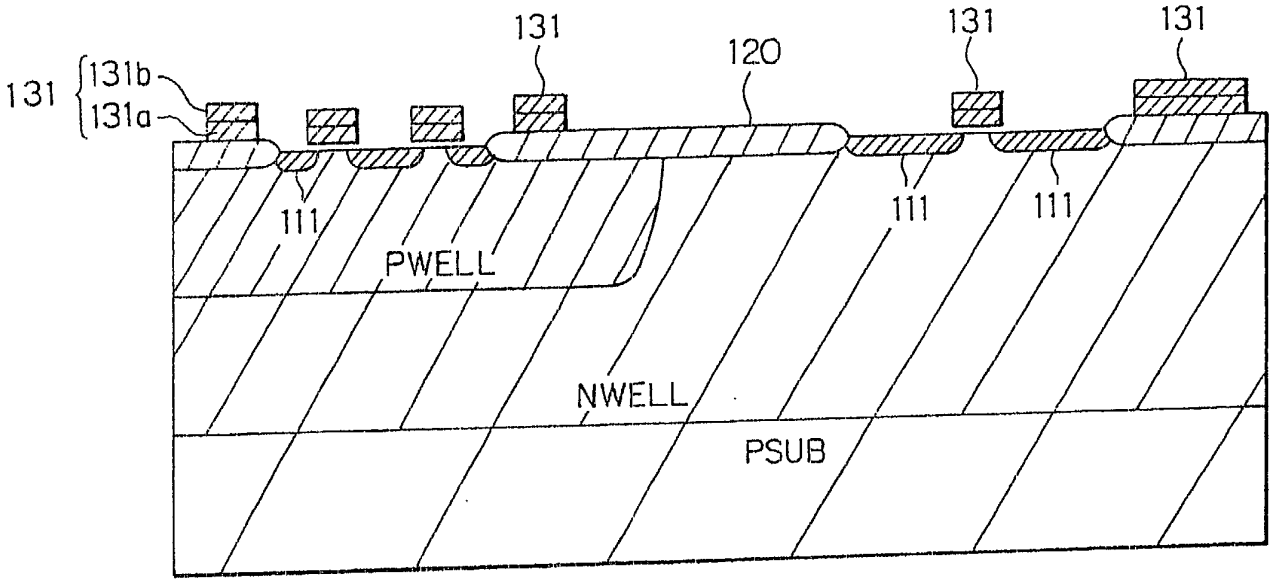


FIG. 5
PRIOR ART

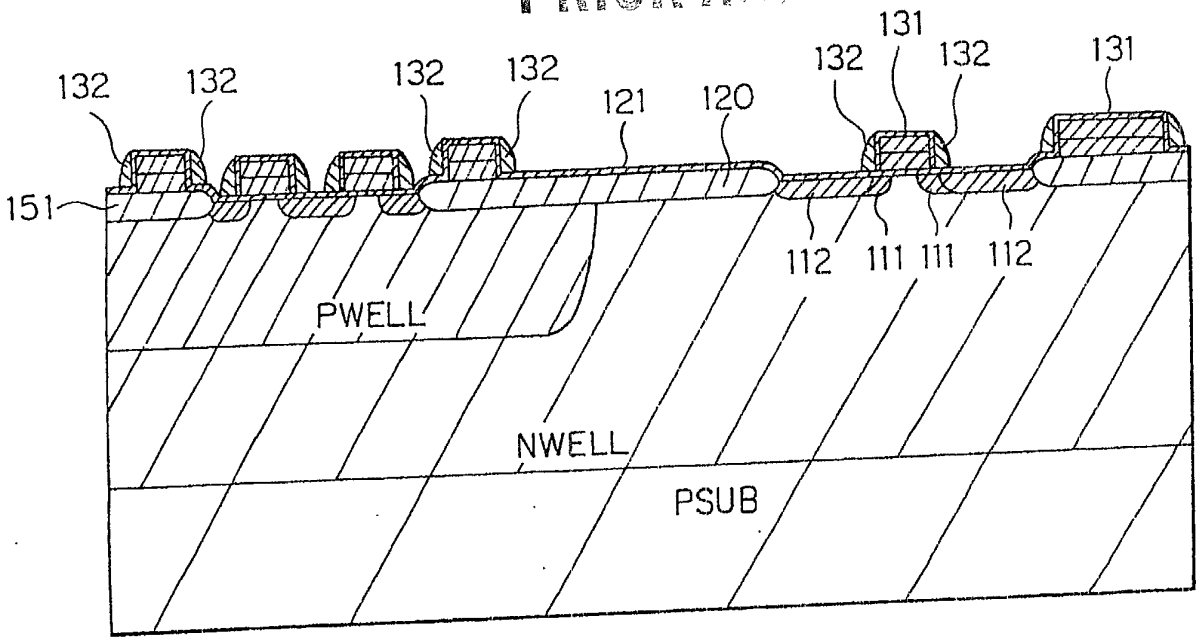


FIG. 6

PRIOR ART

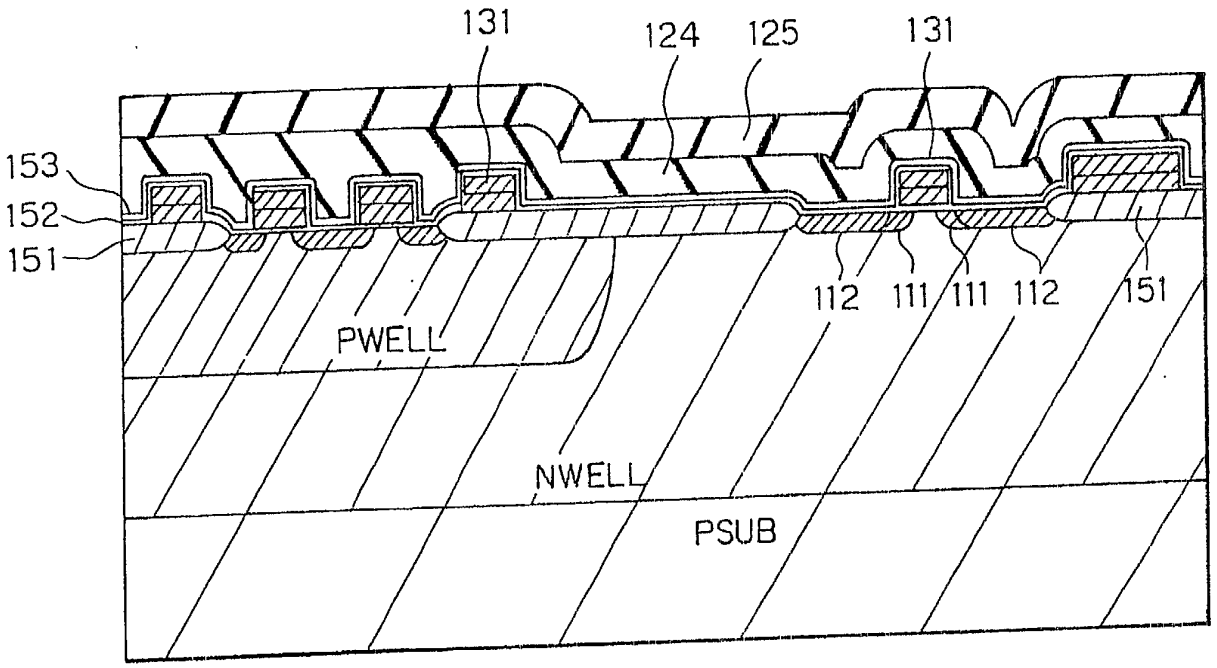


FIG. 7
PRIOR ART

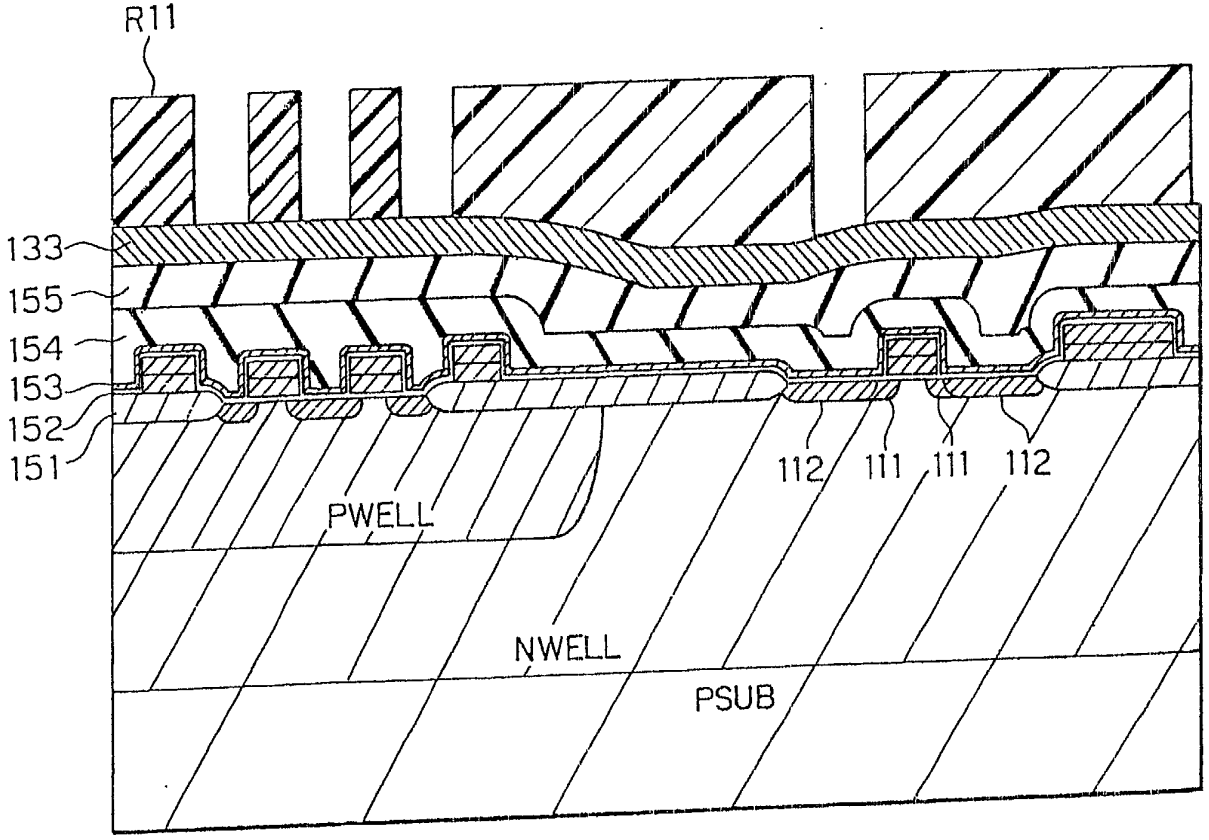


FIG. 8
PRIOR ART

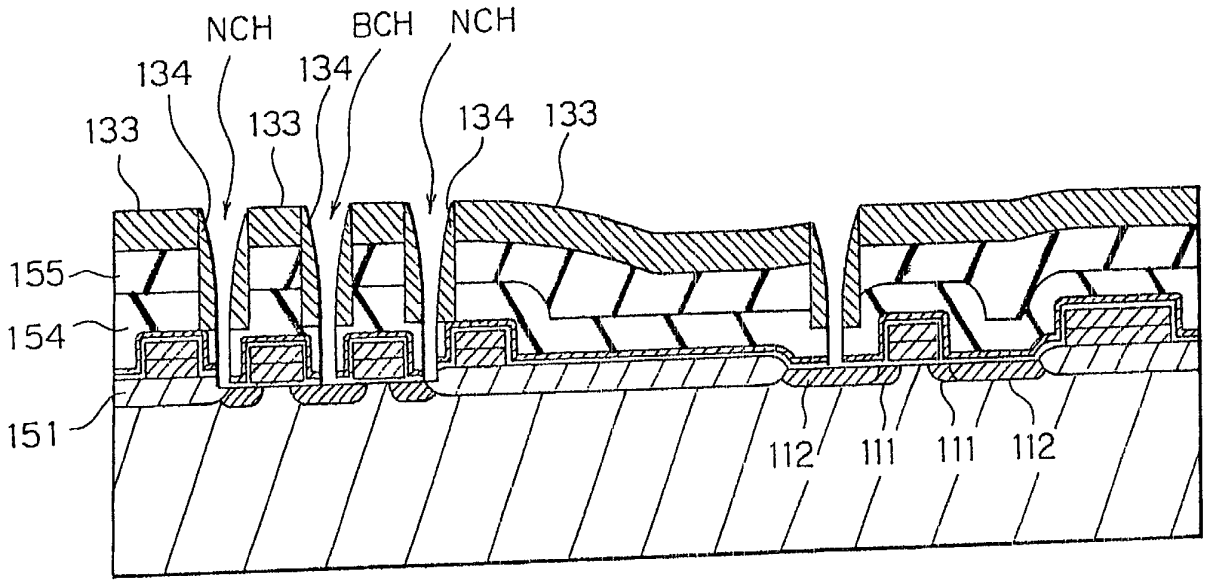


FIG. 9
PRIOR ART

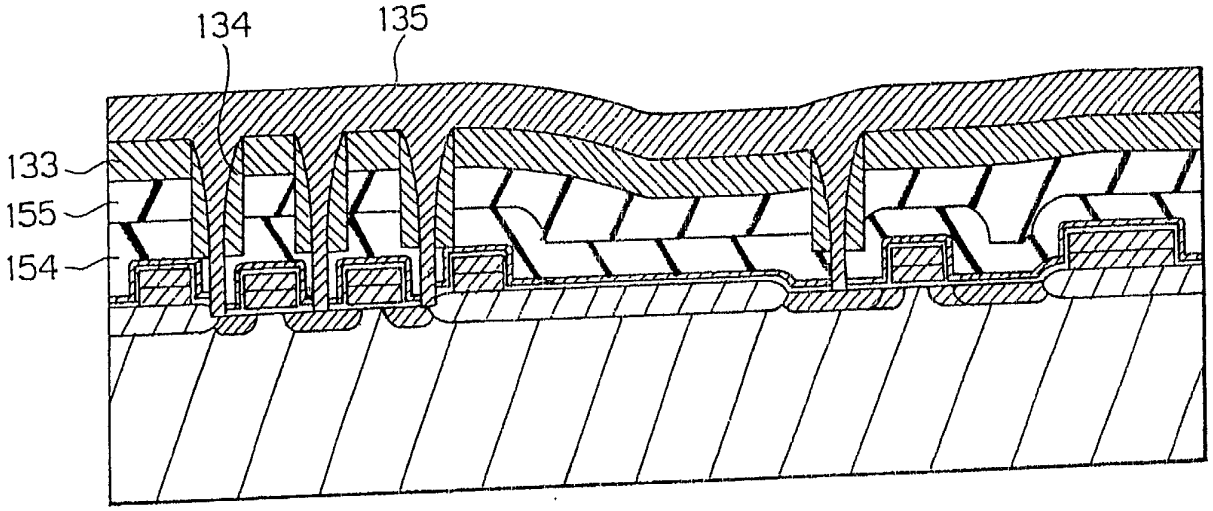


FIG. 10
PRIOR ART

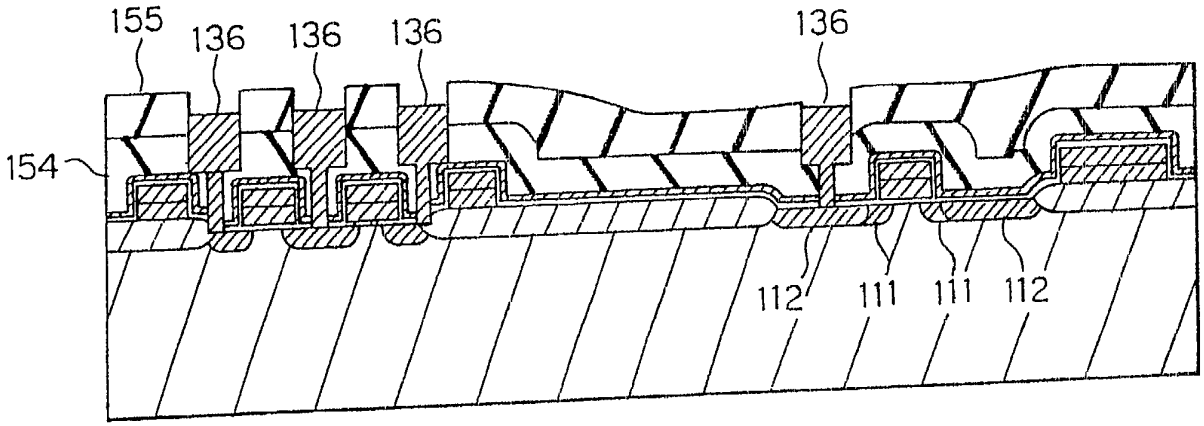


FIG. 11
PRIOR ART

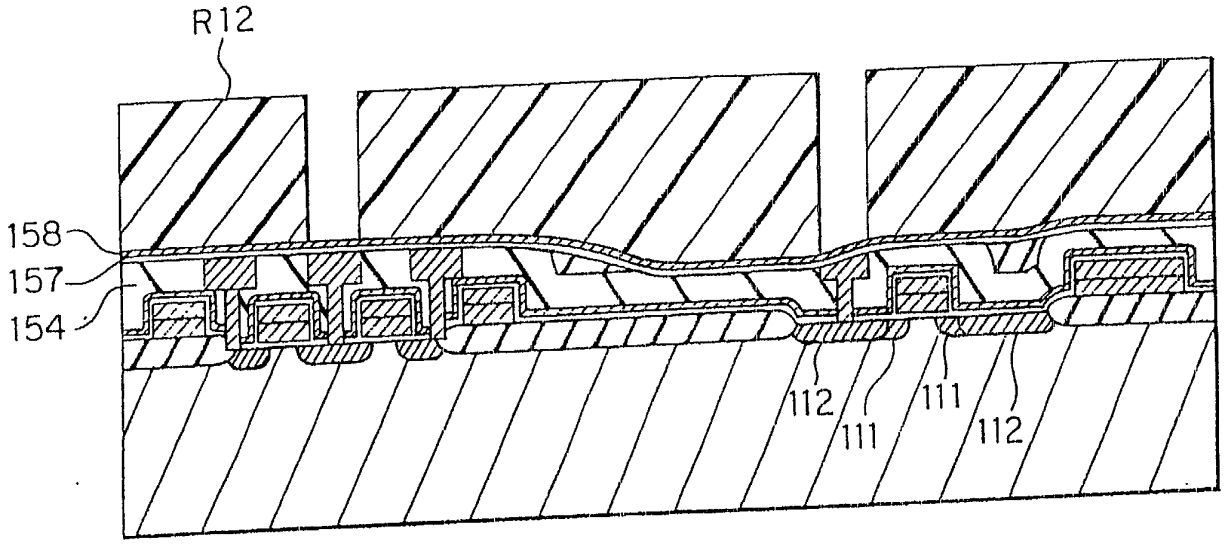


FIG. 12

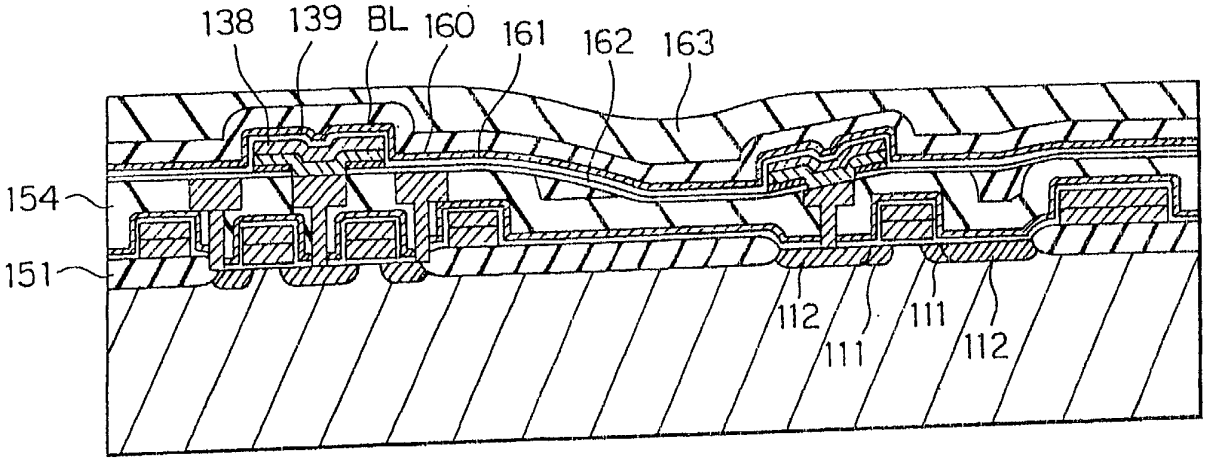


FIG. 13
PRIOR ART

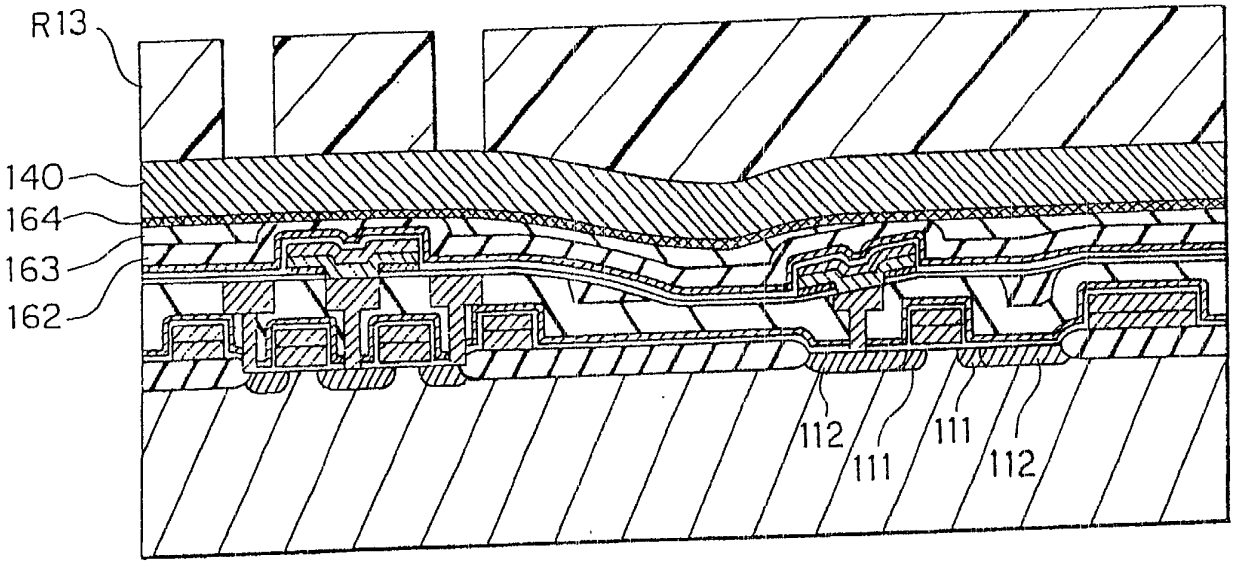


FIG. 14
PRIOR ART

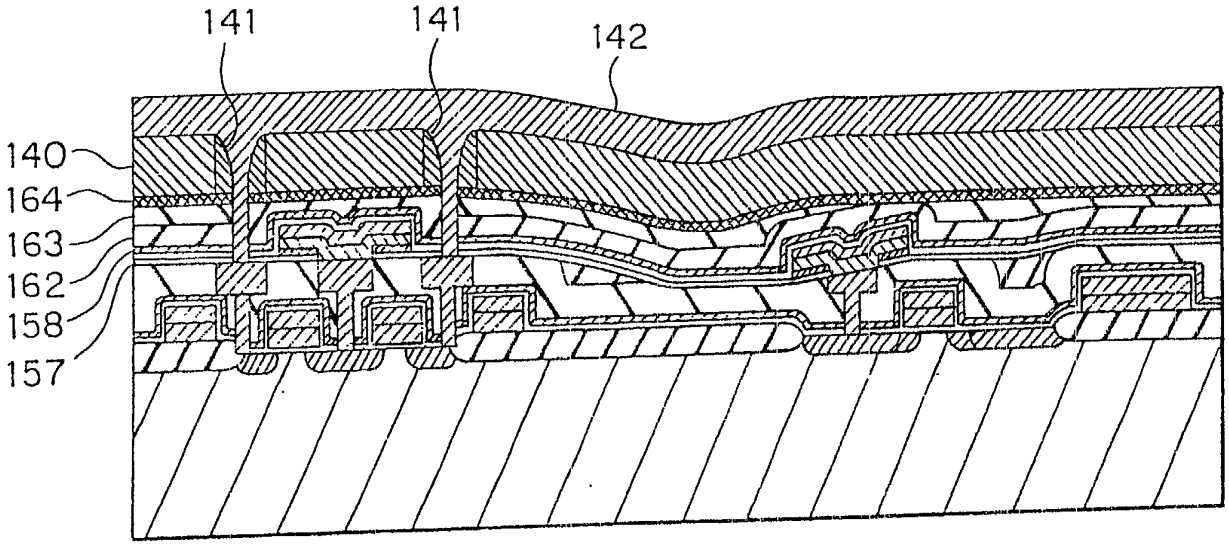


FIG. 15
PRIOR ART

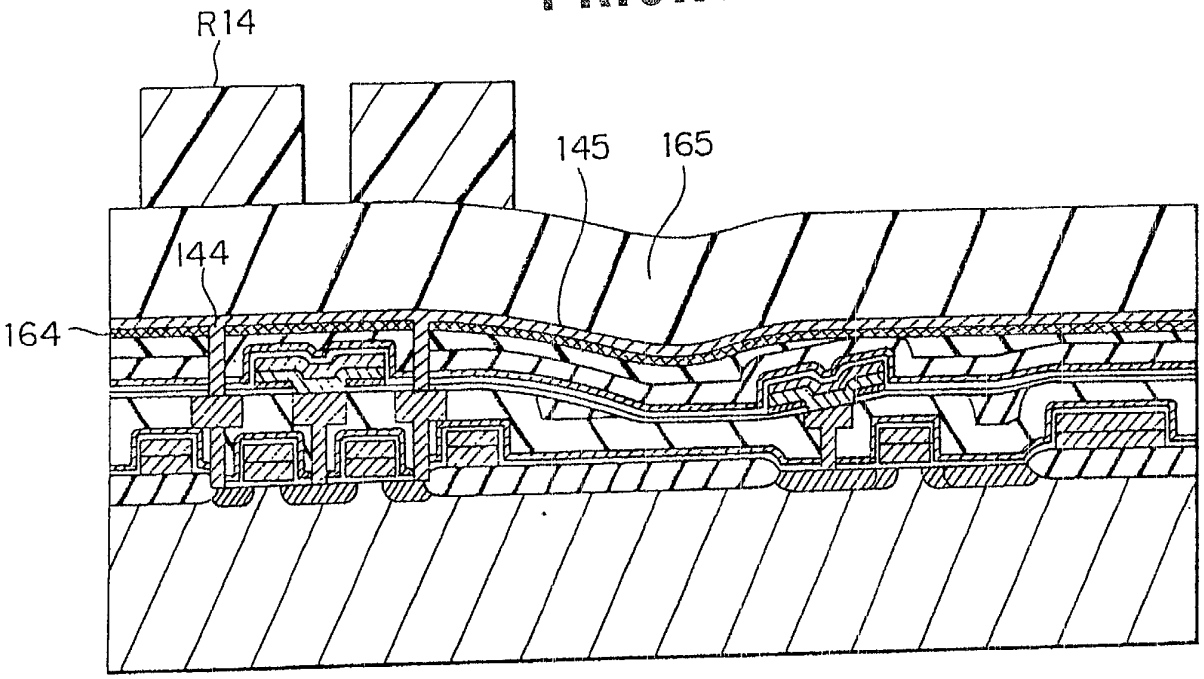


FIG. 16
PRIOR ART

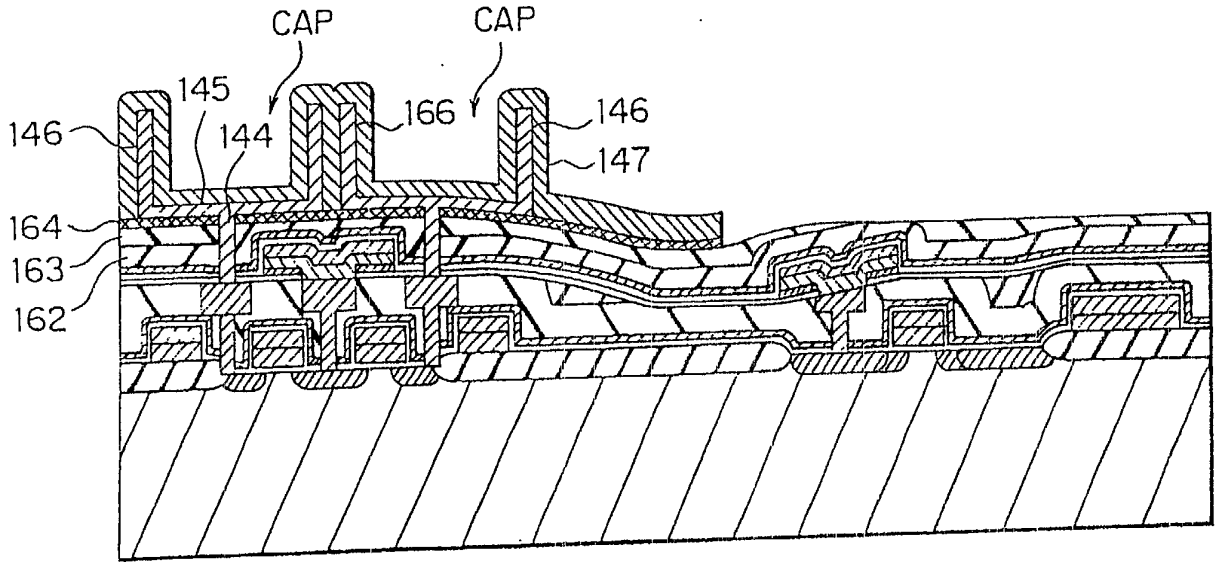


FIG. 17
PRIOR ART